

RC5 receiver core

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This core decodes serial data received from an infrared remote control using the RC5 protocol. It is a fully synchronous design, and uses a clock divider to generate the baud rate. The system clock frequency must be provided using the `clk_freq` parameter.

It features a minimal CPU interface:

- The core implements one register on the CSR that contains the received RC5 code. The register is 13-bit wide, and contains the 14-bit RC5 code stripped of its first start bit.
- An interrupt line is pulsed every time a new RC5 code is received.

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