

FastMemoryLink utilization and performance meter

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1 Introduction

This cores provides a means to extract some statistical parameters about the performance of a memory system based on FastMemoryLink (FML):

- the **net bandwidth** carried by the link (based on the amount of data that the link has actually transferred)
- the **average memory access time**, which is the time, in cycles, between the request being made to the memory controller and the first word of data being transferred.
- the **bus occupancy** which is the percentage of time during which the link was busy and therefore unavailable for a new request.

The design of this core is extremely small and simple. It only requires monitoring two signals of the FML bus: **stb** and **ack**. All the core does is count the number of cycles during which these signals were active during a given time period. Software can then derive the parameters using the equations described below.

The core is controlled via a CSR interface.

2 Register map

Register	Description
0x00	When this register has value 1, the two counters are enabled and are incremented at each cycle the FML strobe and acknowledgement signals are respectively active. Writing 1 atomically resets the two counters and allows them to count. Writing 0 atomically freezes the counters' values.
0x04	Number of cycles during which the strobe signal was active (S). This register is read only.
0x08	Number of cycles during which the acknowledgement signal was active (A). This register is read only.

3 Interpreting the data

3.1 Notations

In the equations that follow, the following symbols are used:

- f is the system clock frequency in Hz
- T is the time during which the counters have been enabled
- w is the width of a FML word in bits
- n is the FML burst length
- S is the number of cycles during which the strobe signal was active
- A is the number of cycles during which the acknowledgement signal was active (number of completed transfers)

3.2 Net bandwidth

The net bandwidth is given by:

$$\frac{w \cdot n \cdot A}{T}$$

3.3 Average memory access time

In FML, a master is waiting when the strobe signal is asserted but the acknowledgement signal is not. Therefore, the total number of wait cycles is given by $S - A$.

The average memory access time can thus be computed as:

$$\frac{S - A}{A}$$

3.4 Bus occupancy

In FML, the bus is busy when the strobe signal is asserted. The bus occupancy is therefore given by:

$$\frac{S}{T \cdot f}$$

3.5 Avoiding overflows

The counters for S and A use 32-bit unsigned values and therefore may overflow and wrap if they are left running for too long. This condition must be avoided as it will lead to incorrect reports.

The worst case for causing overflows is a bus which is always busy (the strobe signal is active at all cycles). Therefore, overflows will be avoided if the following condition is met:

$$T \cdot f < 2^{32}$$

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